Intel® Xeon™ Processor with 512 KB L2 Cache Thermal Models User's Guide

Application Note

January 2002

Contents

Revision History

Rev. No.	Description	Date
2.0	• Initial Release.	January 2002

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1 Introduction

The Intel® Xeon™ processor with 512 KB L2 cache thermal models in Flotherm* and Icepak* are intended for system thermal solution evaluation only. The dimensions and thermal properties in the models are based on estimates only and are subject to change. Refer to the Intel Xeon processor with 512 KB L2 cache datasheet for case temperature and power dissipation specifications.

Users should disregard the temperature gradients within the package itself. Intel strongly recommends that users re-mesh the model according to the accuracy requirements of their system thermal model. No boundary conditions are defined in the models. Users are expected to set the appropriate boundary conditions in the system level thermal model.

1.1 Related Documents

The following documents are useful in the thermal modeling of the Intel Xeon Processor.

Table 1. Related Documents

Document Name	Order Number
Intel® Xeon™ Processor with 512 KB L2 Cache Datasheet	298642
Intel® Xeon™ Processor Thermal Design Guidelines	298348

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2 Thermal Model Usage Guidelines

2.1 Introduction

The Intel® Xeon™ processor with 512 KB L2 cache package thermal models in Flotherm* 2.2 and Icepak* Version 3.1 format are created to assist OEMs in developing their system level thermal solutions. It is strongly recommended that users read this user's guide before using the models.

2.2 Components of the Models

2.2.1 Flotherm* Format

The model is provided as a library file (Intel_Xeon_512K_Flotherm_r20.library). The model consists of the following components:

1. **Package block:** Simulates the thermal behavior of the processor package region. This block includes the pin region of the package.

2. **Cover Assembly block:** This assembly consists of 5 blocks namely "Cover Top" and "Cover L1" through "Cover L4". These 5 blocks represent the integrated heat spreader (IHS) on the processor. The OEM cooling solution must be attached to the top surface of the IHS to ensure proper cooling of the processor package.

3. **Package Power block:** This is a planar heat source called Power. In the model, a 1W power source is provided as an illustration. Users should refer to the latest version of the *Intel® Xeon™ Processor with 512 KB L2 Cache Datasheet* and apply the correct package power dissipation to this source before using this model in their simulations.

2.2.2 Icepak* Format

The model is provided as a compressed zip file (Intel_Xeon_512K_Icepak_r20.zip) containing the necessary files that make up an Icepak* job. The model consists of the following components:

1. **Package block:** Simulates the thermal behavior of the processor package region. This block includes the pin region of the package.

2. **IHS Assembly:** This assembly consists of 5 blocks namely IHS1 through IHS5. These 5 blocks represent the integrated heat spreader (IHS) on the processor. The OEM cooling solution must be attached to the top surface of the IHS to ensure proper cooling of the processor package.

3. **Package Power block:** This consists of one planar heat sources Power to which 1 W has been assigned in the model. Users should refer to the latest version of the *Intel® Xeon™ Processor with 512 KB L2 Cache Datasheet* and apply the correct package power dissipation to this source before using this model in their simulations.

2.3 Modeling Assumptions

1. The entire heat dissipation from all the components within the package is removed through the top of the IHS.
2. Natural convection and radiation inside the package are not considered, because of their minimal impact to heat sink design.
3. Internal components of the package are not included in the model and are simulated using the package keep out block to provide its general system behavior.

2.4 Inserting the Processor Thermal Model into a System Model

2.4.1 Flotherm* Format

1. Load your system level project into Flotherm* Version 3.1 and click on “External”.
2. From the Tool Bar select “Libraries” and set the library type to “Assemblies”.
3. Click on “Import” and select the library file Intel_Xeon_512K_Flotherm_r20.library from the directory where you saved it. Click “OK”. The package assembly is loaded and is called XEON512KPKG-Rev2.0. Click “Dismiss”.
4. In the Project Manager screen, right click “Root Assembly”, select “Location” and the select “Library”. Choose the XEON512KPKG-R20 library, which should appear in the list of libraries. Now click “Load”.
5. The processor package assembly should now be part of your project. You may have to translate and re-orient the assembly to fit your system configuration.
6. If you have any questions regarding this procedure, please contact your customer support representative at Flomerics*.

2.4.2 Icepak* Format

1. Extract the files from Intel_Xeon_512K__Icepak_r20.zip to your hard disk in a directory Start up Icepak*.
2. Load your system level model into Icepak*.
3. Click on Merge job. Select the XEON512KPKG-Rev20 job from the menu. You may have to navigate to the correct top-level directory within which the directory called XEON512KPKG-Rev20 is located. Now click Accept to merge the Prestonia package model into your system level model.
4. The default group for objects from the merged model is merge.0.
5. Go to Groups under Model and use the translate, and rotate features to correctly orient the Prestonia package in your system level model.

6. If you have any questions regarding this procedure, please contact your customer support representative at Fluent Inc.

2.5 Model Limitations

The model is designed for external system level thermal evaluations only. After the package model has been inserted into the system model, the temperature of the geometric center of the top surface of the IHS (Tcase) must be maintained at or below the temperature specification provided in the processor datasheet. Refer the to the processor datasheet or thermal design guidelines for more detailed information on Tcase.